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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/539,334	06/15/2005	Geetha Arthanari	BUR920020005US1	7342
32074 7590 12/18/2006 INTERNATIONAL BUSINESS MACHINES CORPORATION DEPT. 18G BLDG. 300-482 2070 ROUTE 52 HOPEWELL JUNCTION, NY 12533			EXAMINER PARIHAR, SUCHIN	
			ART UNIT	PAPER NUMBER
			2825	
SHORTENED STATUTORY PERIOD OF RESPONSE		MAIL DATE	DELIVERY MODE	
3 MONTHS		12/18/2006	PAPER	

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary

Application No.

10/539,334

Applicant(s)

ARTHANARI ET AL.

Examiner

Suchin Parihar

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 10/5/2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1, 4-5 and 9 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1, 4-5 and 9 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

This FINAL office action is in response to application 10/539,334, amendment filed on 10/5/2006. Claims 2-3, 6-8 and 10 are cancelled. Claims 1, 4-5 and 9 are currently amended. Claims 1, 4-5 and 9 are pending in this application.

Applicant's arguments filed 10/5/2006 have been fully considered but they are not persuasive. The applicable rejections from the prior office action have been incorporated herein.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. **Claims 1 and 9 are rejected under 35 U.S.C. 103(a)** as being unpatentable over Carrig et al. (5,339,253) in view of Zhu (5,866,924).

3. With respect to claim 1, Carrig teaches: collecting a set of sink locations in a master list (i.e. creating a list of sinks to be connected which includes sink locations, Col 2, lines 32-35); selecting a temporary insertion point (i.e. establishing a driving point, Col 2, lines 40; the TIP and the driving point both effectively start the branching process as described on page 3 of Applicant's specification); removing the first subset from the master list (i.e. removing the paired sinks from the list of sinks, Col 2, lines 47-48);

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assigning a first-level structured clock buffer (i.e. a buffer circuit can be added at the sink, Col 6, lines 40-45); repeating steps (a), (b) and (c) for the remaining sinks in the first-level of buffers and subsequent levels until the root level is reached (i.e. repeating steps until the list of sinks contains only a single sink to be connected to each signal [i.e. root level], Col 2, lines 49-52); connecting the root level TIP to lower levels (i.e. using driving points to create another level of the distribution tree, Col 7, lines 15-22); and connecting a source of clock signals to the root level (i.e. connecting single sink to the source, Col 2, lines 53-54). Carrig does not teach: a set of blocked areas; enclosing the sink at the first level furthest from the TIP; and improving the symmetry of the tree by moving SCB locations within constraints to concentrate SCBs in rows and columns. However, Zhu teaches: a set of blocked areas (i.e. obstacle 572 of Figure 5C); enclosing the sink at the first level furthest from the TIP (i.e. branch is formed between the clock source and the clock sink that is farthest from the source, Col 6, lines 25-30); and improving the symmetry of the tree by moving SCB locations within constraints (i.e. symmetric fashion, creating design constraints, Col 2, lines 45-50) to concentrate SCBs in rows and columns (i.e. finding a path for horizontal and vertical wires that will avoid any obstacles, Col 8, lines 28-35). It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate Zhu into the invention of Carrig for the following reason(s): Zhu would improve the skew-controlled distribution network of Carrig by spacing clock sinks in a symmetric fashion, which, as Zhu suggests in Col 2 lines 45-50 would minimize (i.e. control) clock skew. For article of manufacture in

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computer readable form, see Carrig, Col 11, lines 12-20, data input device and/or program storage.

4. With respect to claim 9, Carrig in view of Zhu teaches all the elements of claim 1, from which the claim depends. Carrig teaches: said SCB assigned to a subset of sinks is selected from a set of pre-designed SCBs of varying capacity (a buffer is added at one or both of the sinks to drive them, and this effectively changes both the latency requirements and input capacitance of the sinks, Col 5, lines 45-50, wherein the buffer's pre-designed capacities have an effect on the sinks by changing their requirements).

5. **Claims 4 and 5 are rejected under 35 U.S.C. 103(a)** as being unpatentable over Carrig et al. (5,339,253) in view of Zhu (5,866,924) and in further view of Bergeron et al. (6,609,228).

6. With respect to claim 4, Carrig in view of Zhu teaches all the elements of claim 1, from which the claim depends. Carrig in view of Zhu fails to teach: attempting to place a horizontal SCB then attempting to place a vertical SCB in a central location when a horizontal SCB will not fit in said central location (i.e. adjusting positions [vertical and horizontal] of clock feeding circuits with design constraints to further reduce said lengths of said wires, Col 8, lines 54-58). It would have been obvious to one of ordinary skill in the art to incorporate Bergeron into the inventions of Carrig and Zhu for the following reason(s): the optimization method of Bergeron would improve Carrig and Zhu by providing a method to cluster clocked devices in a way that decreases overall power consumption.

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7. With respect to claim 5, Carrig in view of Zhu and in further view of Bergeron teaches all the elements of claim 4, from which the claim depends. Bergeron teaches: said vertical SCB comprises a set of circuit elements laid out to have substantially the same delay as a corresponding SCB with horizontal layout (i.e. achieving a uniform delay to all latch clusters, Col 3, lines 50-55).

Response to Arguments

8. Applicant asserts that neither Carrig nor Zhu teach, either singly, or in combination, the "connecting steps of claim 1. That is, Applicant asserts that neither Carrig nor Zhu teaches: connecting the root level TIP to lower levels; and connecting a source (S) of clock signals to the root level TIP. Examiner disagrees with this assertion.

9. Examiner points out that Carrig teaches: connecting (i.e. wire up drive points [root levels] with sinks, see Fig 10A of Carrig, #24) the root level Tip to lower levels (additional drive points, thus creating another level of the distribution tree, suggesting that the drive point [root level] will connect to lower level sinks below in the distribution tree, see Col 7, lines 20-25). Also, Carrig teaches: connecting a source (S) of clock signals to the root level TIP (connect drive point [root level TIP] to signal source [source of clock], see Fig 10A, #22).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within

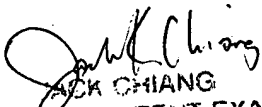
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TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suchin Parihar whose telephone number is 571-272-6210. The examiner can normally be reached on Mon-Fri, 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


JACK CHIANG
SUPERVISORY PATENT EXAMINER


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